REMARKS

Claims 1-20 are pending in the current application. Claims 1, 7, 10 and 20 are independent claims.

35 U.S.C. § 112

Claims 1-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection appears to be based on the preamble language which recites "[a] processor having a processor core and at least one peripheral device" as recited in independent claim 1 and similarly recited in independent claim 7. The Examiner notes that a peripheral device, such as a liquid crystal display (LCD) panel, is not typically positioned within a processor.

Applicant has presently amended the preambles of both independent claims 1 and 7, to recite "[a] processor having a processor core and connected to at least one peripheral device" in claim 1 and similarly recited in claim 7. Applicant respectfully submits that the presently recited preamble language is technically accurate.

Applicants respectfully requests that the Examiner withdraw this rejection.

35 U.S.C. § 103(a) – Kim in view of Johnson

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Johnson. Applicant respectfully traverses this art grounds of rejection.

Kim is directed to a circuit and method of generating clock signals for a low power consumption CDMA modem chip design. In particular, Kim discloses a second clock generator 120 outputting a lower frequency clock signal CLOCK2 to a multiplexer 160 (e.g., see Figure 2 of Kim). The multiplexer 160 also receives a clock signal CLOCK1 at a higher frequency than the clock signal clock 2. The multiplexer 160 receives a clock selection

signal from a clock selection unit 140. The selection signal received from the clock selection unit 140 is based on instructions received from a first clock controller 130.

In response to a power-down instruction, Kim teaches switching a clock signal provided to a processor from the higher frequency clock signal CLOCK1 to the lower frequency clock signal CLOCK2. Initially, Applicant agrees with the Examiner in that Kim:

> does not teach that the selecting circuit determines the operational state of the processor and outputs the selection signal based on the evaluation of the operational state of the processor. Additionally, Kim does not teach that the processor has a processor core and at least one peripheral device
>
> (see page 4 of the Office Action).

The Examiner seeks to combine Johnson with Kim in order to overcome the above described deficiencies of Kim.

Johnson is directed to an input/output (I/O) based embedded processor clock speed control. Johnson teaches that an I/O processor receives I/O requests from a host operating system via a message based interface (MPT) and routes the received I/O requests to an appropriate lower level processor (see column 2, lines 64-66 of Johnson). The I/O processor maintains a record (e.g., a counter) indicating a number of I/O requests received between interrupts, and the counter is then reset after each interrupt (see column 3, lines 30-55 of Johnson). For each I/O request, the counter is incremented. If, during the interrupt, the counter is determined to be below a threshold, the I/O processor decreases its operating speed. Alternatively, if the encounter is not below the threshold, the I/O processor increases or maintains its operating speed (e.g., see steps 4, 5, 8, 9, 12 and 13 of FIG. 3). The sole determination of whether or not the operating frequency of the I/O processor is adjusted is the number of I/O requests received between interrupts as indicated by the counter. The operating frequency of the counter is adjusted **in response** to the I/O request count, and is not

a determining factor in determining whether to adjust the operating frequency. Indeed, such an operation would be rather circular in nature.

Each of the independent claims has been amended so as to change the language of "operational state or operating frequency" to read simply as "operating frequency". In view of Applicant's remarks above with respect to the teachings of Johnson, Applicant respectfully submits that Johnson cannot disclose or suggest "a selecting circuit for determining an operating frequency of the processor and for outputting a selection signal based on the determination" as recited in independent claim 1 and similarly recited in independent claims 7, 10 and 20.

Accordingly, in view of the Examiner admitted deficiencies of Kim, Applicant respectfully submits that the combination of Kim and Johnson is likewise deficient.

As such, claims 2-6, 8-9 and 11-19, dependent upon independent claims 1, 7 and 10, respectively, are likewise allowable over the combination of Kim and Johnson for at least the reasons given above with respect to independent claims 1, 7 and 10.

Reconsideration and issuance of the present application is respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-20 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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